UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/619,669	07/19/2000	Yasuyuki Morishita	DP-652 US	2152

21254 7590 12/16/2002

MCGINN & GIBB, PLLC
8321 OLD COURTHOUSE ROAD
SUITE 200
VIENNA, VA 22182-3817

EXAMINER	
NGUYEN, DILINH P	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 12/16/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/619,669	MORISHITA, YASUYUKI	
	Examiner	Art Unit	
	DiLinh Nguyen	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☒ Interview Summary (PTO-413) Paper No(s). *10* .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (figs. 5A-5B) in view of Voldman (U.S. Pat. 5945713).

Applicant's Admitted Prior Art (figs. 5A-5B) disclose:

an input/output protection device for a semiconductor integrated circuit having a substrate of a first conduction type, an internal circuit, an input/ output terminal. Electrode wiring, and signal wiring, the protection device comprising:

a first diffusion layer 104 fabricated in a region of the first conduction type of the semiconductor substrate 101, the layer having a second conduction type opposite the first conduction type and being connected to the input/output terminal 107; and

a second diffusion layer of the second conduction type being held at a predetermined potential. Applicant's Admitted Prior Art fail to disclose a third diffusion layer of the second conductive type fabricated at a bottom of the second diffusion layer, the third diffusion layer being connected to the second diffusion layer, the first diffusion layer being circularly enclosed with the second and third diffusion layers.

Voldman discloses a semiconductor device (fig. 8, column 8, lines 30 et seq.) comprising:

a diffusion layer 12 of the second conductive type (N) fabricated at a bottom of a diffusion layer (the diffusion layer above the diffusion layer 12), the diffusion layer 12 being connected to the diffusion layer above it; and

a diffusion layer (the one that connected with VDD) being circularly enclosed with the diffusion layers 12 and the diffusion layer above it to prevent current flow to the n-channel MOSFET driver circuit (column 8, lines 37-39). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Applicant 'sAdmitted Prior Art (figs. 5A-5B) to provide a ESD devices with a guard rings structure to prevent current flow to the n-channel MOSFET driver circuit, as show by Voldman.

- Regarding claim 2, Applicant's Admitted Prior Art (figs. 5A-5B) disclose the first conduction type of the semiconductor substrate includes a diffusion layer 102 and it would have been obvious that the layer 102 having an impurity concentration higher than the substrate.
- Regarding claim 3, Applicant's Admitted Prior Art (figs. 5A-5B) disclose the diffusion layer 102, wherein the impurity concentration of the diffusion layer monotonously decreases in a direction from a surface of the semiconductor substrate to an inner section thereof.
- Regarding claims 4 and 13, it is conventional in the art to find the optimal thickness of the diffusion layer through routine and obvious experimentation. It would have been obvious to one having ordinary skill to find the optimal

thickness of the diffusion layer since it is desirable to form devices that are structurally and electrically sound.

- Regarding claims 5, 14-16 and 27, Applicant's Admitted Prior Art (figs. 5A-5B) disclose a lateral, bipolar transistor including the first diffusion layer as a collector, the second diffusion layers as an emitter, and the region of the first conduction type (P) or the diffusion layer 102 as a base is put to operation.
- Regarding claims 6 and 17-20, Applicant's Admitted Prior Art (figs. 5A-5B) disclose wherein the first and second diffusion layers 104 and 105 are isolated form each other by a device separating isolation layer 103 on a surface of the substrate.
- Regarding claims 7-8 and 24, Applicant's Admitted Prior Art (figs. 5A-5B) disclose the layers 104 and 105 are manufactured with a CMOS gate electrode disposed on a surface of the substrate and obvious in a circular shape.
- Regarding claims 9-10, it would have been obvious and matter of design choice to form the gate electrode is connected to the signal wiring of the internal circuit of the semiconductor IC and fixed to a predetermined potential.
- Regarding claim 11, Applicant's Admitted Prior Art (figs. 5A-5B) disclose the first conduction type is a p type and the second conduction type is an n type; and the predetermined potential is a ground potential.
- Regarding claim 12, it would have been obvious and matter of design choice to one having ordinary skill in the art.

- Regarding claim 21, Applicant's Admitted Prior Art and Voldman disclose the claimed invention and Applicant Admitted Prior Art further disclose a diffusion layer 102 surrounded by the substrate 101 and the first and second regions, wherein the layer 102 has the second conduction type.
- Regarding claim 22, Applicant's Admitted Prior Art discloses an impurity concentration of the layer 102 decreases in a direction away from the first region.
- Regarding claim 23, Applicant's Admitted Prior Art discloses the second region 105 is connected to a first constant electrical potential ground terminal 108.
- Regarding claim 25, Applicant's Admitted Prior Art (figs. 5A-5B) disclose a diffusion region 106 having first conduction type (P) and connected to the ground terminal 9.
- Regarding claim 26, Applicant's Admitted Prior Art discloses an output/ input terminal 107.

Response to Arguments

In response to applicant's argument that it is not obvious to combine Voldman with the prior art of Figs. 5A-5B, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case:

Applicant's Admitted Prior Art fail to disclose a third diffusion layer of the second conductive type fabricated at a bottom of the second diffusion layer, the third diffusion layer being connected to the second diffusion layer, the first diffusion layer being circularly enclosed with the second and third diffusion layers.

Voldman discloses a semiconductor device (fig. 8, column 8, lines 30 et seq.) comprising:

a diffusion layer 12 of the second conductive type (N) fabricated at a bottom of a diffusion layer (the diffusion layer above the diffusion layer 12), the diffusion layer 12 being connected to the diffusion layer above it; and a diffusion layer (the one that connected with VDD) being circularly enclosed with the diffusion layers 12 and the diffusion layer above it to prevent current flow to the n-channel MOSFET driver circuit (column 8, lines 37-39).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Applicant 'sAdmitted Prior Art (figs. 5A-5B) to provide

a ESD devices with a guard rings structure to prevent current flow to the n-channel MOSFET driver circuit, as show by Voldman.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DiLinh Nguyen whose telephone number is (703) 305-6983. The examiner can normally be reached on 8:00AM - 6:00PM (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

DLN
December 7, 2002

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800